Enabling Testability of Fault-Tolerant Circuits by Means of IDDQ-Checkable Voters

ECE 7502 Class Discussion

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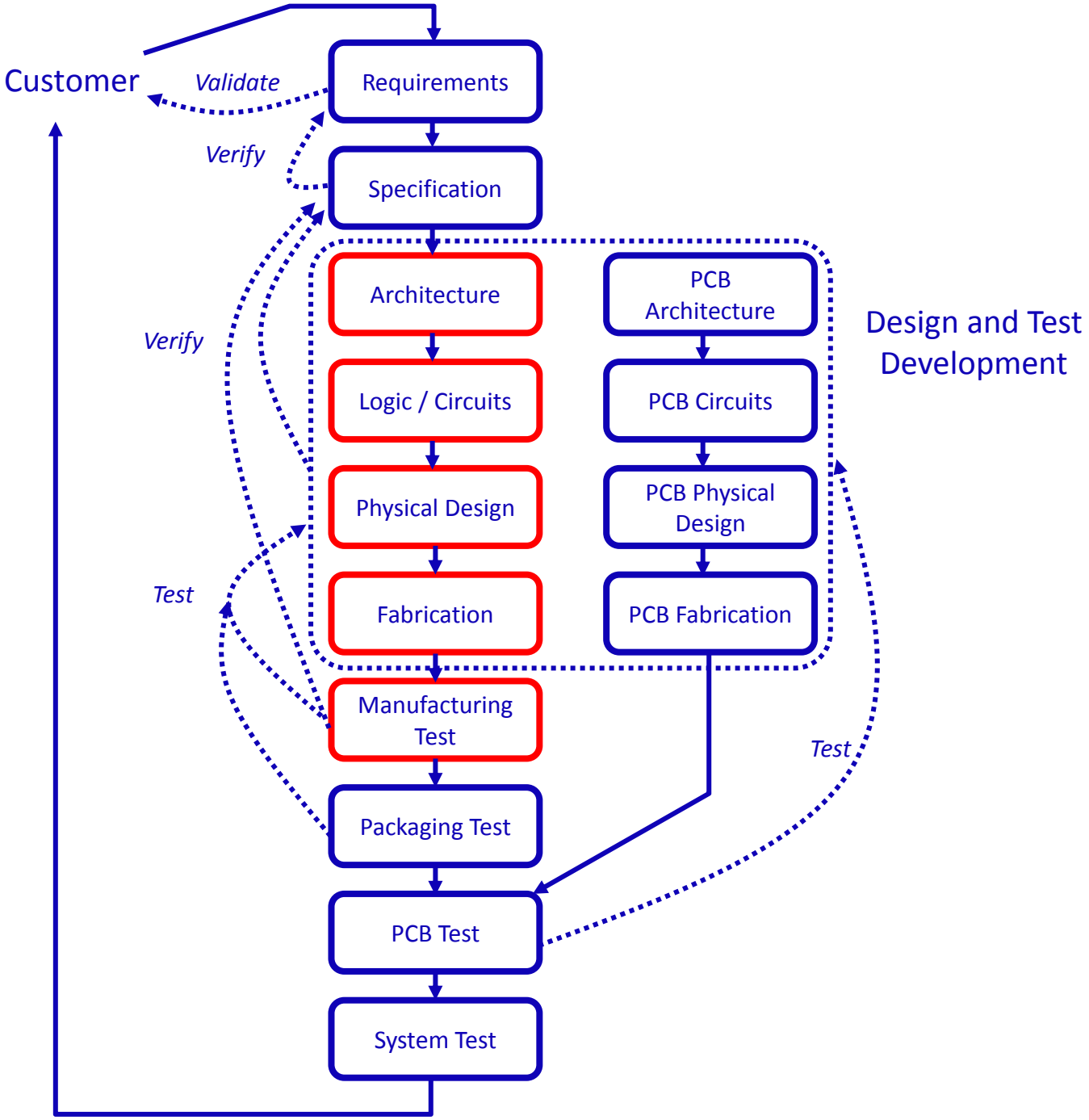
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System Test
PCB Architecture
PCB Circuits
PCB Physical Design
PCB Fabrication
Design and Test Development

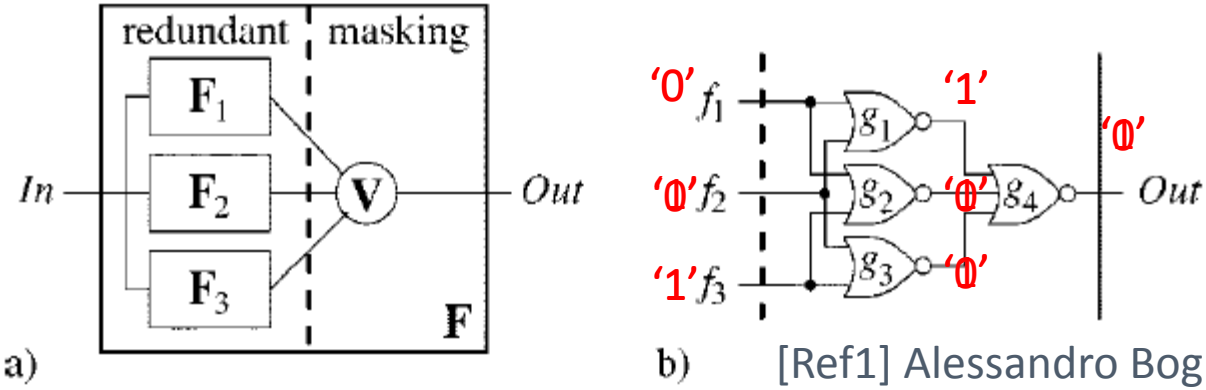
Background

- Fault tolerant design.
  - Systems oriented to highly reliable applications (e.g., space, avionic, vehicle, etc.) will reinforce the use of fault-tolerance design.
  - Redundancy. Hardware redundancy, software redundancy, time redundancy, and a combination of above redundancy.
  - Trade-off between performance and reliability.
- Fault tolerant verification.
  - Faults are to be masked by the fault tolerant design.
  - Fault tolerance impairs testability.

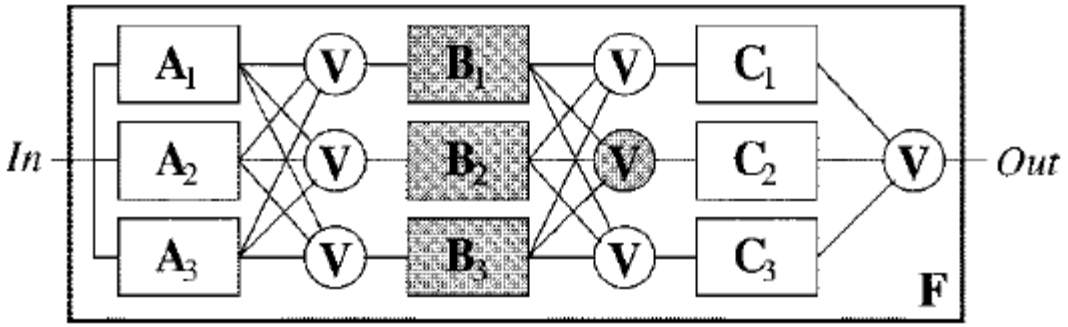
Introduction

- Conventional DFT techniques for fault tolerant circuits requires directly accessible to redundant components.
  - A remarkable increase of the number of I/O pins, or the insertion of built-in self test structures.
  - Do not support on-line testing.
- This paper developed the IDDQ-checkable voters(ICVs), which worked as traditional CMOS voters in fault-free conditions, while they can detect maskable stuck-at faults by monitoring quiescent currents.

Stuck at fault tolerant circuit



[Ref1] Alessandro Bogliolo



- Redundant stage is a redundant implementation of the circuit's functionality.
- Masking stage implements an error-correcting mechanism by **majority voting**.

Testability issues

- Stuck-at fault is detectable if and only if it causes an output error for at least one primary input configuration.
- This paper only consider the fault tolerant circuit whose redundant stage and masking stage are stuck-at testable. That means f1, f2 and f3 has the wrong output if stuck at fault exists in F1, F2 and F3.

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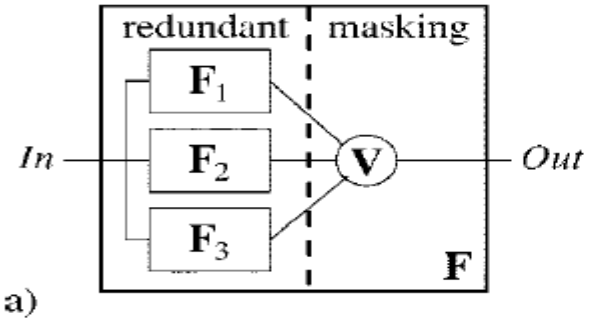
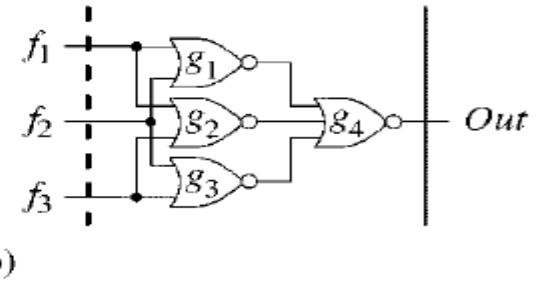




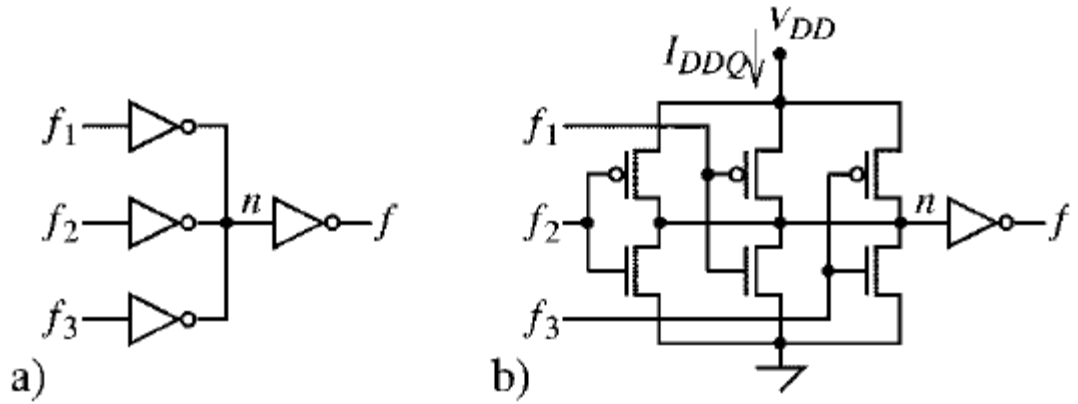
DFT for stuck at fault.

- Conventional DFT techniques
  - 1) Adding observation/control points at the outputs of the replicated modules
  - 2) Making independently controllable the inputs of the functional modules
- Holdbacks of above techniques
  - Not practical when dealing with multilevel fault tolerant circuits due to excessive hardware overhead required to bypass multiple masking stages and propagate error-detecting signals to outputs.
  - Fault masking should be disabled during the testing.

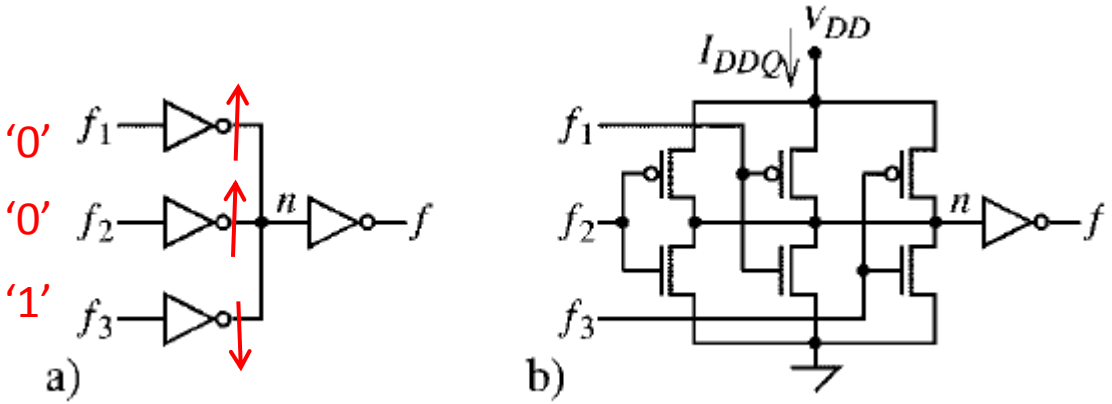
IDDQ Checkable Voters

- Assumption: Any maskable fault of the redundant stage propagates to the inputs of a voting elment.
- Property: Necessary and sufficient information to detect any possible maskable fault is available at the masking stage.

[Ref1] Alessandro Bogliolo



IDDQ Checkable Voters



[Ref1] Alessandro Bogliolo

ICV mechanism:

- Voting result is decided by the number of 1 and 0 in f1, f2 and f3.
- The voltage of node n is affected by f1, f2 and f3, and there is on current if stuck-at fault exists.
- IDDQ test can be used to detect on current resulted from stuck-at.

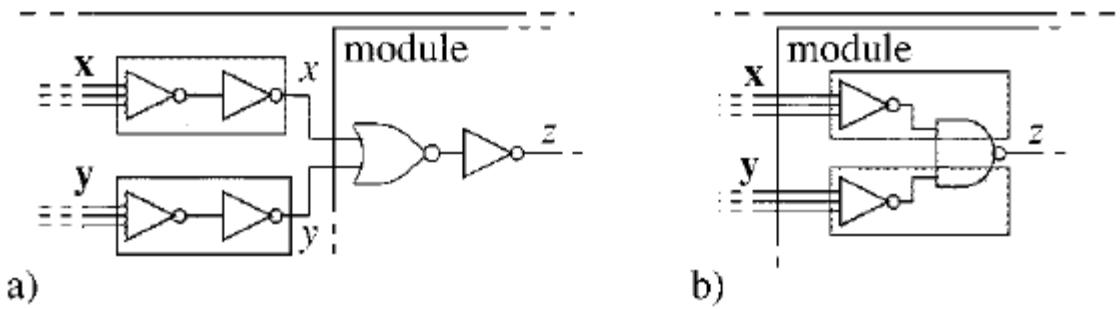
Advantages:

- Detect stuck-at fault by using IDDQ test.
- On-line testing. Do not require propagation of fault.

Holdbacks:

- Large on current if stuck-at fault exists.
- Noise margin is diminished at node n because of ratio circuits.

Multi level fault tolerant circuits



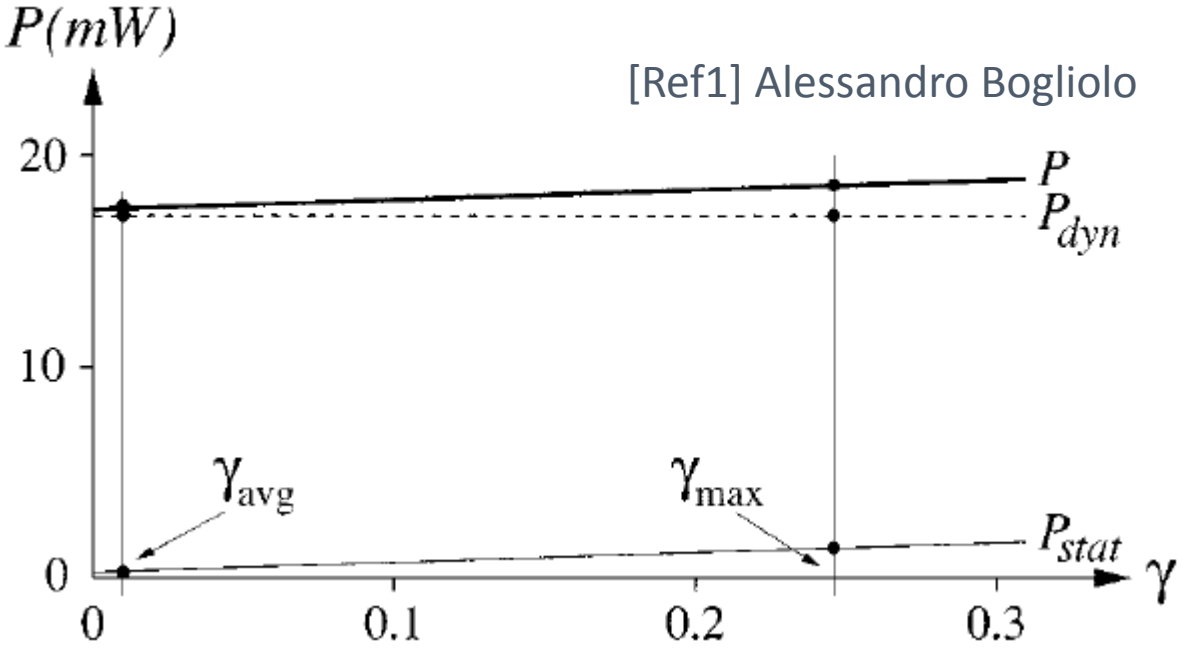
[Ref1] Alessandro Bogliolo

- To achieve testability of maskable faults of a multilevel fault tolerant circuit, every masking stage should use IDDQ-Checkable Voters(ICVs).
- To further reduce hardware overheads, ICVs can be embedded into the functional logic by reducing the stages of logical gates.

Performance evaluation

- Error-free states : all inputs are ‘1’ or ‘0’.
- Error-correcting states: two ‘1’ and one ‘0’ or two ‘0’ and one ‘1’.
  - Static supply current is 220 uA.
  - Voltage of node n is 2.65V and 0.45V.
  - Propagation delay ranges from 0.27ns to 0.45ns. 30% degradation of error correction.
- Simulation environment:
  - 0.3um technology
  - Minimum-size NMOS and double-size PMOS
  - VDD=3.3V
  - CL=25fF

Average power consumption



[Ref1] Alessandro Bogliolo

γ is the average detection probability, which is defined as the percentage of primary input vectors causing an error at the inputs of the ICV. The fault free circuit has γ=0.

Limitations of IDDQ-Checkable Voters

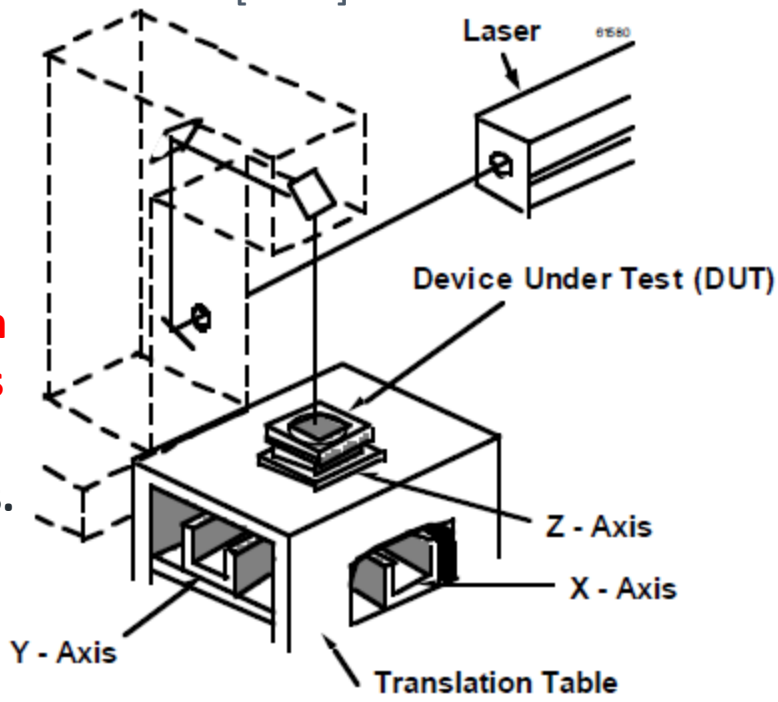
- The leakage current of the entire circuit could hide the IDDQ due to faults.
- The use of built-in current sensor may impair performance.

Another technique: Laser fault injection

- *Laser Fault Injection (LFI) technique to inject soft, i.e., transient, faults into VLSI circuits in a precisely-controlled, non-destructive, non-intrusive manner for the purpose of validating fault tolerant design and performance.*

[Ref2] John R. Samson

The principle behind the laser injection technique is the generation of carriers in the silicon substrate which then collect in a diffusion area of the target circuit. Absorption of the laser energy creates electron-hole pairs in a manner similar to SEU (Single Event Upset) effects caused by high energy particles. If charge collects in the diffusion area of a CMOS transistor, a momentary change in logic output can occur.



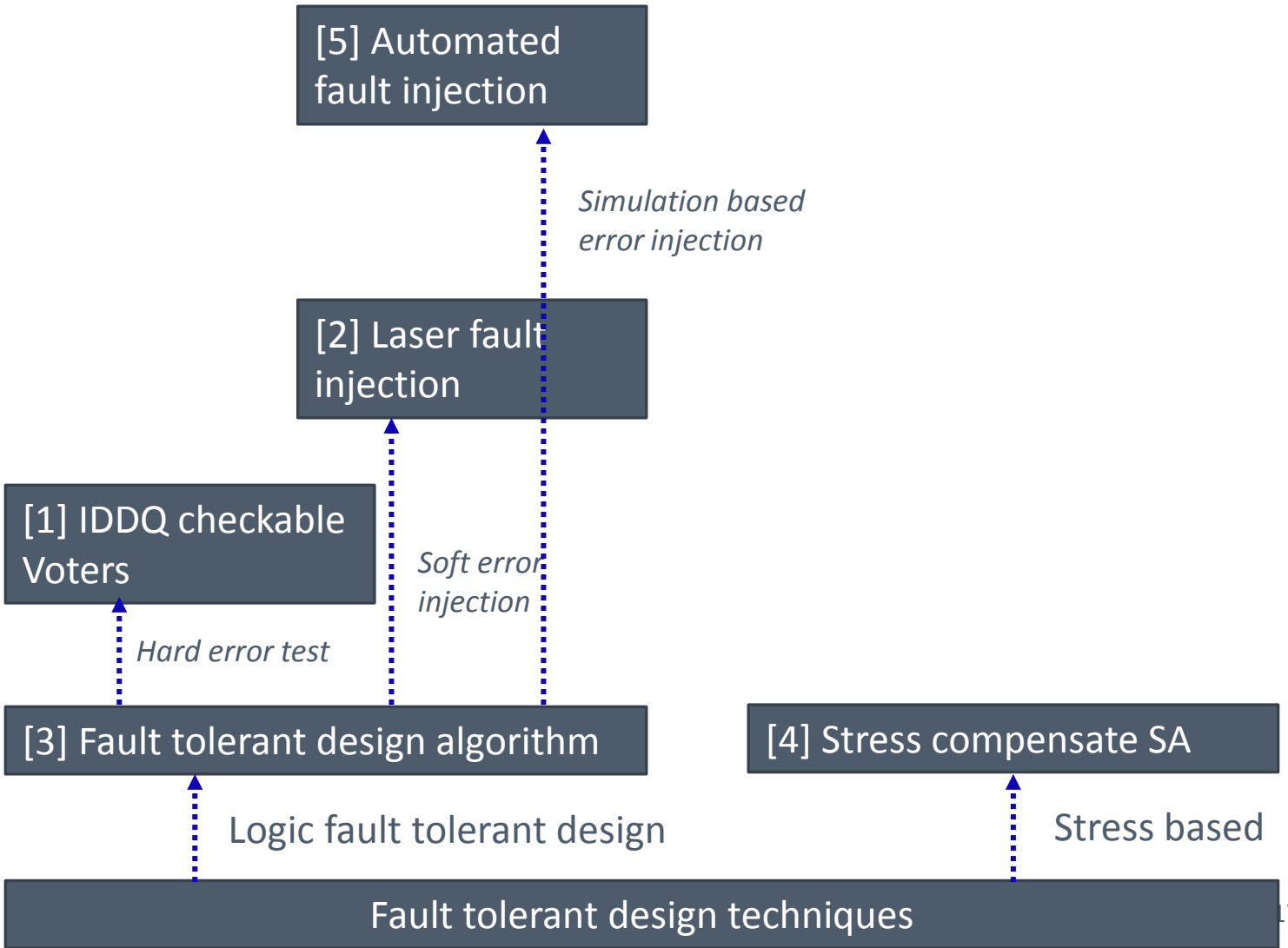
Discussion questions

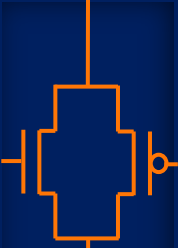
1. Why fault tolerant impairs testability and why it is necessary to assess reliability?
2. Why the circuit is no longer FT and its reliability may become even lower than that of a (simpler) non-FT implementation once a permanent maskable fault has occurred?
3. Why maskable faults are inherently undetectable?
4. What is the benefit of online testing?
5. Why we do not need to inhibit the fault-masking mechanism during the testing phase, if fault detection is based on IDDQ testing that does not require fault propagation?

Papers

- [1] Alessandro Bogliolo, Michele Favalli, and Maurizio Damiani. "Enabling Testability of Fault-Tolerant Circuits by Means of IDDQ-Checkable Voters", IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 8, NO. 4, AUGUST 2000.
- [2] John R. Samson, Jr, "A Technique for Automated Validation of Fault Tolerant Designs Using Laser Fault Injection (LFI)," , Fault-Tolerant Computing, 1998. Digest of Papers. Twenty-Eighth Annual International Symposium on DOI: 10.1109/FTCS.1998.689466.
- [3] Kshirsagar, R.V. ; Patrikar, R.M, "A novel fault tolerant design and an algorithm for tolerating faults in digital circuits," Design and Test Workshop, 2008. IDT 2008. 3rd International. DOI: 10.1109/IDT.2008.4802486.
- [4] Beshay, P. ; Bolus, J. ; Blalock, T. ; Chandra, V. ; Calhoun, B.H, "SRAM sense amplifier offset cancellation using BTI stress," Subthreshold Microelectronics Conference (SubVT), 2012 IEEE. DOI: 10.1109/SubVT.2012.6404299.
- [5] Aleksandar Simevski, Rolf Kraemer1, and Milos Krstic, "Automated Integration of Fault Injection into the ASIC Design Flow," Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), 2013 IEEE International Symposium on. DOI: 10.1109/DFT.2013.6653615.

Paper Map (e.g.)


[5] Automated fault injection
Simulation based error injection
[2] Laser fault injection
[1] IDDQ checkable Voters
Soft error injection
Hard error test
[3] Fault tolerant design algorithm
[4] Stress compensate SA
Logic fault tolerant design
Stress based
Fault tolerant design techniques



Glossary

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